## **AMENDMENTS TO THE CLAIMS**

1. (currently amended) A memory subsystem with symbol sliced command repowering comprising: a command register in operable communication with a plurality of memory devices via a plurality of command buses; wherein said plurality of memory devices is arranged into symbol slices and each symbol slice is configured to be part of a single error correction code packet; and a memory controller, said memory controller in operable communication with said command register including a command bus employing an error correction code; wherein each command bus of said plurality of command buses is configured to interface between said command register and each memory device in a particular symbol slice. 2. (cancelled) 3. (cancelled) 4. (cancelled) 5. (original) The memory subsystem of Claim 1 further including a memory interface device in operable communication with said plurality of memory devices and said memory controller, with at least one of a command bus between said memory controller and said memory interface and a command bus between said memory interface and said command register including a command bus employing an error correction code.

6. (original) The memory subsystem of Claim 1 wherein said plurality of

memory devices and said command register comprise a dual in line memory module.

## 7. (cancelled)

- 8. (currently amended) The memory subsystem of Claim 7-1 further including a memory interface device in operable communication with said plurality of dynamic random access-memory modules devices and said memory controller, with at least one of a command bus between said memory controller and said memory interface and a command bus between said memory interface and said command register including a command bus employing said another error correction code.
- 9. (currently amended) The memory subsystem of Claim 7–8 wherein said plurality of memory devices and said command register comprise a dual in line memory module.
- 10. (currently amended) The-A method of implementing command bus redundancy in a memory subsystem comprising:

configuring a plurality of memory devices into symbol slices, each symbol slice configured to be part of a single error correction code packet;

establishing configuring a plurality of command buses, each command bus configured to interface with each memory device in a particular symbol slice; and

configuring a command register with sufficient command bus drivers to support each command bus of said plurality of command buses configuring a memory controller in operable communication with said command register including a command bus employing an error correction code.

- 11. (cancelled)
- 12. (cancelled)

- 13. (currently amended) The method of Claim 10 further including eommunicating configuring a memory interface device in communication with said plurality of memory devices and said memory controller, with at least one of a command bus between said memory controller and said memory interface and a command bus between said memory interface and said register including a command bus employing an error correction code.
- 14. (currently amended) The method of Claim 10 wherein said plurality of memory devices and said command register comprise a dual in line memory module.
- 15. (currently amended) The method of Claim 10 further including:

  communicating configuring a command register in communication with a plurality of memory devices;
- eommunicating configuring said a memory controller with said command register, said communicating including a command bus employing another error correction code.
- 16. (currently amended) The method of Claim 15 further including eommunicating configuring a memory interface device in communication with said plurality of memory devices and said memory controller, with at least one of a command bus between said memory controller and said memory interface and a command bus between said memory interface and said register including a command bus employing said error correction code.
- 17. (currently amended) A system for command bus redundancy in a memory subsystem comprising:
- a means for configuring a memory device array configured into symbol slices, each symbol slice configured to be part of a single error correction code packet;

a means for establishing a plurality of command registers each including a plurality of command buses associated therewith, each command bus configured to interface with each memory device included within a particular symbol slice; and a means for configuring a command register with sufficient command bus drivers to support each command bus of said plurality of command buses a memory controller, said memory controller in operable communication with said plurality of command registers including a command bus employing an error correction code.